

ABSTRACT OF DISCLOSURE

A method of fabricating a TFT using dual or multiple gates, and a TFT having superior characteristics and uniformity by providing a method of fabricating a TFT using dual or multiple gates by calculating the probability including N_{max} , the maximum number of crystal grain boundaries in active channel regions according to the length of the active channels, and adjusting a gap between the active channels capable of synchronizing the number of the crystal grain boundaries in each active channel region of the TFT using the dual or multiple gates in the case where G_s , the size of crystal grains of polycrystalline silicon forming a TFT substrate, θ angle in which "primary" crystal grain boundaries are inclined at a direction perpendicular to an active channel direction of the gates, the width of the active channels and the length of the active channels are determined.